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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/484,311	01/18/2000	James John Casto	1001-0087	9539
22120	7590	01/14/2004	EXAMINER	
ZAGORIN O'BRIEN & GRAHAM, L.L.P. 7600B N. CAPITAL OF TEXAS HWY. SUITE 350 AUSTIN, TX 78731			LEE, EUGENE	
			ART UNIT	PAPER NUMBER
			2815	

DATE MAILED: 01/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

'Office Action Summary	Application No.	Applicant(s)	
	09/484,311	CASTO ET AL.	
	Examiner	Art Unit	
	Eugene Lee	2815	<i>MLW</i>

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 October 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 2-12, 15-25 and 27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 2-12, 15-25 and 27 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____ |

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DETAILED ACTION

In view of the appeal brief filed on 10/2/03, PROSECUTION IS HEREBY REOPENED.

A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 2 thru 6, 10, 11, 17, 18, 22, and 23 are rejected under 35 U.S.C. 103(a) as obvious over Macpherson et al. 6,369,437 B1 in view of Andoh 6,674,163. MacPherson discloses (see, for example, Figure 1) fuses (programmable elements) formed in an integrated circuit device. In Figure 1, Macpherson discloses a fuse (programmable element) 1 being coupled to a signal line (power supply voltage node). A second fuse (second programmable element) 3 is coupled to

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a different signal line (second power supply voltage node). A middle fuse has two nodes (internal package node) that couple a second end of fuse 1 to a second end of fuse 3.

Macpherson does not disclose a package for mounting at least one integrated circuit die.

However, it was well known in the art at time of invention to put dies in packages in order to protect the die and have it function properly. Andoh discloses (see, for example, Fig. 10) a chip 52 in a package 51. The package molds the chip and protects it from the outside environment. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to include a package in order to protect the integrated circuit device and have it function properly.

Regarding claim 5, a photoresist layer 21 covers the fuse.

Regarding claim 6, MacPherson discloses the claimed invention except for the programmable element not being covered by a protective layer. However, not covering the programmable element makes a cheaper and easier to produce semiconductor device. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to exclude the protective layer, in order to make a cheaper and more easily produced semiconductor device, and since it has been held that omission of an element and its function in a combination where the remaining elements perform the same function as before involves only routine skill in the art. In re Karlson, 136 USPQ 184.

3. Claims ⁽²⁾2, 7 thru 9, 11, ⁽¹²⁾12, 15 thru ⁽¹⁷⁾18, 20 thru ⁽²¹⁾23 and 27 are rejected under 35 U.S.C. 103(a) as obvious over Crafts et al. 5,536,968 in view of Andoh 6,674,163 B1. Crafts discloses (see, for example, FIG. 3) a fuse array PROM comprising fuse structures 10 wherein a

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first and second end is coupled to V_{DD} , external I/O terminals or resistors 40. In FIG. 3, Crafts discloses two fuses 10 that lie on a fourth row of the PROM fuse array. Each fuse is coupled to a different V_{DD} power supply. A second end of one of the fuses 10 is coupled to a second end of the other fuse 10 by way of a node (black dot, internal package node). Crafts does not disclose a package for mounting at least one integrated circuit die. However, it was well known in the art at time of invention to put dies in packages in order to protect the die and have it function properly. Andoh discloses (see, for example, Fig. 10) a chip 52 in a package 51. The package molds the chip and protects it from the outside environment. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to include a package in order to protect the integrated circuit device and have it function properly.

4. Claim 12 is rejected under 35 U.S.C. 103(a) as obvious over Hamdy et al. 5,266,829 in view of Andoh 6,674,163 B1. Hamdy discloses (see, for example, FIGURE 5a) anti-fuses formed for an integrated circuit PROM. In FIGURE 5a, Hamdy discloses anti-fuse (programmable element) 168d being coupled to a bit line (power supply voltage) 00. Anti-fuse (another programmable element) 168h is coupled between a second end of anti-fuse 168d and output (external package connection) 178. Hamdy does not disclose a package for mounting at least one integrated circuit die. However, it was well known in the art at time of invention to put dies in packages in order to protect the die and have it function properly. Andoh discloses (see, for example, Fig. 10) a chip 52 in a package 51. The package molds the chip and protects it from the outside environment. Therefore, it would have been obvious to one of ordinary skill in the

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art at the time of invention to include a package in order to protect the integrated circuit device and have it function properly.

5. Claim 21 is rejected under 35 U.S.C. 103(a) as obvious over Best 5,748,031 in view of Andoh 6,674,163 B1. Best discloses (see, for example, FIG. 2) a semiconductor integrated circuit comprising a fuse (one-time programmable element) 255, V_{SS} (power supply voltage node), fuse (another one-time programmable element) 245, and external pad (external package connection) 260. A node (internal package node) lies adjacent to pad 265 in between pads 245, 255. Best does not disclose a package for mounting at least one integrated circuit die. However, it was well known in the art at time of invention to put dies in packages in order to protect the die and have it function properly. Andoh discloses (see, for example, Fig. 10) a chip 52 in a package 51. The package molds the chip and protects it from the outside environment. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to include a package in order to protect the integrated circuit device and have it function properly.

6. Claims 19 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacPherson et al. '437 B1 in view of Andoh '163 B1 as applied to claims 2-6, 10, 11, 17, 18, 22, and 23 above, and further in view of Hall '632 B1. MacPherson does not disclose the integrated circuit die including a processor wherein the processor is programmed (to perform various functions) by programmable elements. However, Hall discloses (see, for example, FIG. 3) a fuse array ^{304 - 306} 202, 204, 206, a processor and clock source. Hall discloses that the fuse array specifies the operating characteristics of the processor (i.e. clock frequency). Therefore it would have been

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obvious to one of ordinary skill in the art at the time of invention to use the fuses of Macpherson in order to specify the operating characteristics of a processor.

7. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over MacPherson et al. '437 B1 in view of Andoh '163 B1 as applied to claims 2-6, 10, 11, 17, 18, 22, and 23 above, and further in view of Barth, Jr. et al. '616. MacPherson does not disclose an error correction code (ECC). However, Barth, Jr. discloses (see, for example, column 12, lines 10-34) a semiconductor memory device wherein fuses are programmed to perform an error correction. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to program the fuses of Macpherson and use them for error correction in order to remove the effects of bad bit lines in a memory device.

Response to Arguments

8. Applicant's arguments with respect to claims 2-12, 15-25, and 27 have been considered but are moot in view of the new ground(s) of rejection.

INFORMATION ON HOW TO CONTACT THE USPTO

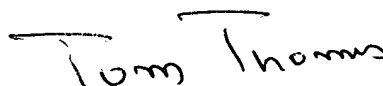
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 703-305-5695. The examiner can normally be reached on M-F 8-5.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Eugene Lee
January 12, 2004

A handwritten signature in black ink that reads "Tom Thomas". The signature is written in a cursive, slightly stylized font.

TOM THOMAS
SUPERVISORY PATENT EXAMINER